STRUCTURE OF SEMICONDUCTOR ELECTRONIC DEVICE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to a semiconductor electronic device typified by MOSFET or the like, and particularly to a structure suitable for use in a semiconductor electronic device using an SOI substrate and a method of manufacturing it.

Description of the Related Art:

According to a reference: "SIMOX-LSI Technology Latest Report" by High-Technology Promotion Institute Corp., p 220, issued in 1998 (in the tenth year of Heisei), attention has been focused on an electronic device formed over an SOI (Silicon On Insulator) substrate as a device having excellent characteristics such as low power consumption, speeding-up, etc. Various element technologies about the design, production, etc. of the electronic device have been studied together with a wafer manufacturing technology. As shown in the reference, a process for forming silicides has been widely used to reduce sheet resistances of source and drain regions and a gate electrode region of a transistor.

However, the silicides have features that they are selectively formed by reaction with a metal and Si alone and they will not be formed without reaction with the

metal and SiO_2. Since a micro device is short in gate length, silicides are grown so as to seat below or get under side walls formed over side walls of a gate electrode upon formation of the silicides in its source and drain regions, and they reach near a gate oxide film. Thus, this will create problems such as an increase in gate leakage current, a reduction in gate withstand voltage, a short channel effect, etc.

SUMMARY OF THE INVENTION

In order to solve the above-described problems, an object of the present invention is to provide a structure suitable for use in a semiconductor electronic device, wherein each of side walls provided over sides of a gate electrode of a field effect transistor formed over a substrate has a structure convex toward the substrate side, and silicides are formed over a source and drain of the field effect transistor and a gate electrode thereof and not grown to the portion under the side walls of the gate electrode.

Further, the present invention provides a structure suitable for use in a semiconductor electronic device, wherein side walls composed of silicides, which are lower than side walls formed on the sides of a gate electrode of a field effect transistor formed over a substrate, are formed in contact with the side walls formed on the sides thereof, and silicides are

respectively formed over a source, a drain and the gate electrode of the field effect transistor and not grown to the portion under the side walls of the gate electrode.

Furthermore, the present invention provides a method of manufacturing a semiconductor electronic device, which is capable of easily forming the above structure in a simple process.

Typical ones of various inventions of the present application have been shown in brief. However, the various inventions of the present application and specific configurations of these inventions will be understood from the following description.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects and features of the invention and further objects, features and advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

Fig. 1 is a structure cross-sectional view (1) for describing a first embodiment of the present invention;

Fig. 2 is a structure cross-sectional view (2) for describing the first embodiment of the present invention;

Fig. 3 is a structure cross-sectional view for

describing a second embodiment of the present invention;

Fig. 4 is a process cross-sectional view for describing a third embodiment of the present invention;

Fig. 5 is a process cross-sectional view for describing a fourth embodiment of the present invention;

Fig. 6 a process cross-sectional view for describing a fifth embodiment of the present invention;

Fig. 7 is a process cross-sectional view for describing a sixth embodiment of the present invention; and

Fig. 8 is a process cross-sectional view for describing a seventh embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFFERED EMBODIMENTS

The present invention aims to control the transverse growth of silicides downward of a gate, reduce a gate leakage current, enhance a gate withstand voltage and improve a short channel effect. Further, the present invention is suitable for use in a device using an SOI substrate. However, the present invention can be applied even to a device using a conventional Si substrate and is effective therefor.

Respective embodiments will hereinafter be described in detail with reference to the accompanying drawings.

(First embodiment)

Figs. 1 and 2 are respectively structure cross-

sectional views for describing a first embodiment of the present invention. In a structure suitable for use in a semiconductor electronic device using an SOI substrate, structures convex toward the SOI substrate side are provided below side walls on the sides of a gate electrode after the formation of the gate electrode as designated at symbols a and a' in Fig. 1. The shape of each structure may be accurate. Alternatively, their shapes may be rectangular as designated at symbols b and b' in Fig. 2.

Owing to the provision of the oxide film structures convex toward the SOI substrate sides below the side walls as designated at symbols a and a' in Fig. 1 and symbols b and b' in Fig. 2, the growth of silicides is blocked and thereby stops by oxide films convex toward the substrate side when the silicides are formed over the source, drain and gate of a transistor. Therefore, the silicides do not seat or get under the side walls.

In the structures according to the present invention as shown in Figs. 1 and 2, no silicides dives under the side walls. The resultant device can achieve a reduction in gate leakage current, an increase in gate withstand voltage and an improvement in short channel effect.

(Second embodiment)

Fig. 3 is a structure cross-sectional view for describing a second embodiment of the present invention.

A semiconductor electronic device using an SOI substrate takes a structure wherein as shown in Fig. 3, a gate electrode is formed and thereafter side walls (see c and c' in Fig. 3) composed of silicides are formed outside portions below side walls each comprised of an insulating material, which are formed on the sides of the gate electrode. This structure has a structure wherein side walls each composed of Poly-Si or amorphous Si, i.e., side walls (sub side walls) smaller than the side walls composed of the insulating material in both height and width are first formed outside portions below the side walls each composed of the insulating material, the sub side walls and a metal are allowed to reach with each other so as to be brought into silicidation, and the silicided ones are formed integrally with silicides used for a source and a drain.

When the Poly-Si or amorphous Si is placed in such locations as designated at c and c' in Fig. 3 to thereby form silicides over the source, drain and gate of a transistor, the Poly-Si or amorphous Si placed in such locations as designated at c and c' in Fig. 3 also reacts with a metal simultaneously so as to be brought into silicidation. At this time, the metal, which reacts with Si of the SOI substrate, is etched at the portions designated at c and c', and hence the silicided ones do not grow up to below a gate oxide film. Thus, the silicides do not get under the side walls.

In such a structure as shown in Fig. 3, according to the present invention, no silicides get under the side walls. The resultant device can achieve not only an improvement in gate withstand voltage but also a reduction in gate leakage current. While Fig. 3 shows the case using the SOI structure, the present invention can be of course applied to the conventional Si substrate.

(Third embodiment)

Fig. 4 is a process cross-sectional view for describing a third embodiment of the present invention. As shown in Fig. 4(1), an oxide film (SiO_2) for forming first side walls is formed by a CVD method or the like after the formation of a gate electrode. As shown in Fig. 4(2), side wall etching is effected on the oxide film by dry etching using CF_4 gas or the like. In the present invention, however, etching is excessively effected without increasing a selection ratio at etching, and a trenching effect at each edge is utilized to etch even Si of an SOI layer at the edge. As shown in Fig. 4(3), thermal oxidation is then effected under the same condition as gate oxidation. Thereafter, an oxide film identical in quality to a gate oxide film is formed over the exposed Si portions. Next, side wall formation is executed again as shown in Fig. 4(4) by the CVD method or the like, so that side walls each having a shape convex downwardly toward the SOI layer are formed under the previous side walls. Thereafter, the surface of the SOI

layer and the surface of the gate electrode are allowed to react with a metal so as to be brought into silicidation.

When the silicides are formed over the source, drain and gate electrode through the use of the side wall structure formed by the above-described method, the silicidation at the source and drain is blocked by the oxide film convex downwardly toward the SOI substrate, thus causing no transverse growth of the silicides downward of the gate oxide film.

According to the manufacturing method of the present invention such as shown in Figs. 4(1) through 4(5), the silicides do not get under the side walls. Further, the resultant device allows not only an improvement in gate withstand voltage but also a reduction in gate leakage current. While the present embodiment shows the case using the SOI substrate, it is needless to say that it can be also applied to the conventional Si substrate.

(Fourth embodiment)

Fig. 5 is a process cross-sectional view for describing a fourth embodiment of the present invention. As shown in Fig. 5(1), a gate electrode is formed and thereafter an oxide film (SiO_2) used for first side walls is deposited thereon by a CVD method or the like. Further, as shown in Fig. 5(2), first side wall etching is effected with dry etching using CF_4 gas or the like,

and a trenching effect at each edge is utilized to etch even Si of an SOI layer at the edge. As shown in Fig. 5(3), the exposed Si is further etched by using an Si etching solution such as an ammonia solution of 1-30% or a hydrofluoric acid + hydrogen peroxide solution or the like. Next, as shown in Fig. 5(4), the exposed Si (etched portions) are oxidized to form oxide films identical in quality to a gate oxide film. Next, side walls are formed again as shown in Fig. 5(5). Consequently, portions below the side walls respectively have shapes convex downwardly toward the SOI layer.

When the side wall structure formed by the above-described method is utilized to allow Si to react with a metal for the purpose of forming silicides, the silicides are blocked by the oxide films convex downwardly toward the SOI layer and hence no transverse growth of silicides downward of the gate oxide film occurs. Further, the degree of convexity of the oxide film toward the SOI substrate side can be adjusted by etching before the side walls are formed again by the CVD method or the like. Thus, the present embodiment also has the advantage that the degree of downward convexity of the oxide film can be controlled according to the thickness of each silicide layer.

In the structure of the present invention such as shown in Fig. 5(6), the degree of convexity of the oxide film below each side wall toward the substrate side can

be controlled according to the thickness of the silicides upon formation of the silicides different in thickness from each other. Thus, the silicides do not get under the side walls upon formation of the silicide films different in thickness from each other. The resultant device allows not only an increase in gate withstand voltage but also a decrease in gate leakage current.

(Fifth embodiment)

Fig. 6 is a process cross-sectional view for describing a fifth embodiment of the present invention. SiO_2 A having a thickness of from 5nm to 50nm, which is shown in Fig. 6(1), is formed over an SOI substrate. Thereafter, Poly-Si or amorphous Si B shown in Fig. 6(2) is formed and grooves or trenches each having a width of from 100nm to 500nm are defined in their corresponding positions of side walls to be formed later by the known photolithography and etching. Afterwards, the selective growth of silicon is performed to thereby deposit selectively grown Si C shown in Fig. 6(3) over the Poly-Si or amorphos Si B , whereby the width of each trench is adjusted to a range from 5nm to 100nm. Next, as shown in Fig. 6(4), the Poly-Si or amorphous Si B and the selectively grown Si C are removed by wet or dry etching after the removal of SiO_2 A lying at the bottoms of the trenches. In doing so, the SOI substrate itself is etched simultaneously. When SiO2 A is thereafter removed, extra fine trenches each having a width of from

5nm to 100nm, which cannot be formed by the conventional method, are defined in the SOI substrate as shown in Fig. 6(5). Then, gate oxidation is carried out to form a gate oxide film D shown in Fig. 6(6). Further, a Poly-Si gate E is formed as shown in Fig. 6(7) and side walls F are formed.

When the side wall structure formed by the above-described method is used to form silicides G as shown in Fig. 6(7), the silicides G are blocked by rectangular oxide films convex in the substrate direction, which are located below the side walls. Thus, the silicides do not seat under the side walls F and the resultant device can achieve not only an improvement in gate withstand voltage but also a reduction in gate leakage current. Further, the device also has a feature that since the degree of convexity of the oxide film below each side wall toward the substrate can be controlled by etching, the degree of downward convexity of the oxide film can be controlled according to the thickness of a silicide layer.

In the structure of the present invention as shown in Fig. 6(7), the degree of convexity of the oxide film below each side wall downward of the SOI substrate can be controlled according to the thickness of the silicides upon formation of the silicides different in thickness from each other. The silicides do not get under the side walls upon formation the silicide films different in thickness from each other. Further, silicide edges can

be steeply controlled in the vertical direction along the sides of the side walls. The resultant device can achieve not only an increase in gate withstand voltage but also a decrease in gate leakage current.

(Sixth embodiment)

Figs. 7(1) through 7(5) are respectively process cross-sectional views for describing a sixth embodiment of the present invention. Since the process steps from Figs. 6(1) to 6(4) employed in the fifth embodiment are similar process steps in the present embodiment, their description will be omitted.

After the execution of the process steps shown in Figs. 6(1) through 6(4), trenches each having a width of about 50nm and a depth of from about 5nm to about 50nm are first defined in an SOI substrate as shown in Fig. 7(1). Afterwards, Si is epitaxially grown to deposit epitaxial Si A ' shown in Fig. 7(2) over the SOI substrate. Further, each of the trenches is adjusted to the required width and depth. The depth of each trench is set so as to range from 5nm to 25nm, for example, and the width thereof is set to range from 5nm to the length of the width of a lower portion of each side wall D ' to be formed later. Next, gate oxidation is performed to form a gate oxide film B ' as shown in Fig. 7(3).

Further, when a Poly-Si gate C ' is formed and the side walls D ' are formed as shown in Fig. 7(4), an oxide film structure convex downwardly toward the SOI substrate

is formed below each side wall D '.

According to the above-described method as compared with the fifth embodiment referred to above, it is easy to control the size (width and depth) of each trench shown in Fig. 7(1). Further, the side wall structure convex toward the substrate can be easily formed.

In the structure of the present invention such as shown in Fig. 7(5), the degree of downward convexity of the oxide film below each side wall toward the substrate can be easily controlled according to the thickness of the silicides upon formation of the silicides different in thickness from each other. The silicides do not get under the side walls upon formation the silicide films different in thickness from each other. Further, silicide edges can be steeply controlled in the vertical direction along the sides of the side walls. The resultant device can achieve an increase in gate withstand voltage, and a decrease in gate leakage current and limit a short channel effect.

(Seventh embodiment)

Fig. 8 is a process cross-sectional view showing a seventh embodiment. As shown in Fig. 8(1), a gate oxide film A ", a Poly-Si gate electrode B ", and side walls C " are formed in a normal process as shown in Fig. 8(1). Afterwards, Poly-Si or amorphous Si D " is formed. Next, anisotropic dry etching of Si is performed as shown in

Fig. 8(2) to thereby form a structure in which Si D " equivalent to less than or equal to one-half the height of each side wall C " is left behind.

When silicides E " are formed through the use of the side wall structure formed by the above-described method, silicides as designated at D " are formed even outside the side walls as shown in Fig. 8(3). However, no silicides are formed below the gate oxide film A ". This is why since the Poly-Si or amorphous Si D " rather than Si of an SOI substrate is easy to silicide, the lower sides of the side walls C " are not silicided.

In such a construction of the present invention as shown in the final structure shown in Fig. 8(3), the transverse and inner growth of silicides downward of the gate oxide film A " does not occur. Further, the resultant device can be improved in gate withstand voltage and reduced in gate leakage current and can limit a short channel effect.

It is needless to say that the device structures and manufacturing methods described in the first through seventh embodiments can be applied to a normal Si substrate similarly to the SOI substrate.

While the present invention has been described with reference to the illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the